In the Claims:

Please amend claims 1, 6, and 12 as follows, and add new claims 13 and 14:

1. (Thrice Amended) A method of manufacturing a semiconductor integrated circuit comprised of a plurality of functional blocks and a gate array block, each of the plurality of functional blocks being respectively provided with predetermined functions by semiconductor devices, the method comprising the steps of:

c8 placing the gate array block comprised of a plurality of basic cells arranged in line and the plurality of functional blocks within a predetermined first area including a center position on a surface of a semiconductor chip, the gate array block and the plurality of functional blocks being formed on the surface of the semiconductor chip with a common mask;

placing a plurality of I/O buffers in a second area surrounding the first area;

designing circuits for inclusion in the gate array block; and

establishing electrical connections between the basic cells within the gate array block by using interconnections according to the circuits designed in the previous step.

6. (Thrice Amended) A semiconductor integrated circuit comprising:

a plurality of functional blocks placed on a semiconductor chip, said functional blocks being respectively provided with predetermined functions by semiconductor devices;

c9 a gate array block placed on said chip, said gate array block being comprised of a plurality of basic cells arranged in line and electrically connected between the basic cells lying within the gate array block by interconnections implementing a desired function, the gate array block having a circuit designed after placing said plurality of functional blocks and said plurality of basic cells on said chip,

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wherein said functional blocks and said gate array block are laid out with a common mask in a first area including a center position on a surface of the semiconductor chip; and

a plurality of I/O buffers surrounding the first area.

12. (Twice Amended) A method of manufacturing a semiconductor integrated circuit comprising a plurality of functional blocks and a gate array block, each of said plurality of functional blocks being respectively completed by a layout design, the method comprising the steps of :

placing the gate array block, comprised of a plurality of basic cells arranged in line, within a first area of a semiconductor chip and said plurality of functional blocks within a second area of said semiconductor chip, the gate array block and the plurality of functional blocks being formed on the surface of the semiconductor chip with a common mask;

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placing a plurality of I/O buffers in a third area surrounding the first and second areas;

designing circuits for inclusion in the gate array block; and

establishing electrical connections between the basic cells lying within the gate array block by using interconnections in accordance with the designed circuits whereby said designed circuits are formed on said semiconductor chip.

13. (New) The method of manufacturing a semiconductor integrated circuit of claim 1, wherein the electrical connections are formed with a circuit mask.

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14. (New) The method of manufacturing a semiconductor integrated circuit of claim 12, wherein the electrical connections are formed with a circuit mask.